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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,155	10/25/2001	Sailesh Kottapalli	42P12494	7078

8791 7590 06/02/2005

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EXAMINER

TRIMMINGS, JOHN P

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/033,155

Applicant(s)

KOTTAPALLI ET AL.

Examiner

John P. Trimmings

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 August 2004.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 August 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

PD

DETAILED ACTION

This Office Action is in response to the applicant's amendment dated 8/16/2004.

The applicant amended Claims 1, 10 and 14.

Claims 1-17 are pending.

Response to Amendment

1. In view of the replacement drawings submitted 8/16/2004, the examiner withdraws the objections to said drawings.
2. In view of the applicant's argument, the examiner recognizes the applicant right to omit a Summary of the Invention in the Disclosure.
3. In view of the amendment to Claim 14, the examiner withdraws the rejection of said claim under 35 USC 112 first paragraph.
4. In view of the amendments to independent Claims 1 and 10, the applicant's arguments, filed 8/16/2004, with respect to the rejections of claims 1-13 under 35 USC 102 and 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Cohen (see below).
5. In view of the amendment to independent Claim 14, the examiner maintains the rejection of Claims 14-17 made under 35 USC 102(e) to Phan in the Office Action of 5/13/2004. Applicant should submit an argument under the heading "Remarks" pointing out disagreements with the examiner's contentions. Applicant must also discuss the

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references applied against the claims, explaining how the claims avoid the references or distinguish from them.

Claim Rejections - 35 USC § 103

6. Claims 1, 2, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure, U.S. Patent No. 5666482, and further in view of Cohen et al., U.S. Patent No. 5692152.

As per Claim 1:

McClure teaches an apparatus comprising: a processor (column 10 lines 22-23), coupled to a cache memory (column 10 lines 20-21); the cache memory with a plurality of cache lines (column 8 line 44), each cache line with at least one status bit to represent whether the cache line contains a defect (column 8 lines 59-61); and a logic to perform at least one test of the plurality of cache lines and to set the status bit for at least one of the plurality of cache lines (column 8 lines 53-61). However, McClure fails to further teach, at least one valid bit to indicate whether the line is valid. But in the analogous art of Cohen et al., this feature is disclosed in column 1 lines 56-67. And in column 2 lines 48-53, the advantage of the invention is higher speed access to cache data through a master-slave system. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include the master-slave system including validity tagging of cache data in order to increase cache data access speed.

As per Claim 2:

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McClure further teaches the apparatus of claim 1 wherein the logic is a programmable built in self-test (PBIST) logic (column 10 lines 3-4). And in view of the motivation previously stated, the claim is rejected.

As per Claim 5:

McClure further teaches the apparatus of claim 1 wherein the status bit is stored in a register file cell (column 10 lines 1-2). And in view of the motivation previously stated, the claim is rejected.

As per Claim 8:

McClure further teaches the apparatus of claim 1 wherein the cache memory is either one of a level 0 (L0) cache, level 1 (L1) cache, or level 2 (L2) cache (column 10 lines 22-23 and column 2 lines 29-36). And in view of the motivation previously stated, the claim is rejected.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure, U.S. Patent No. 5666482., in view of Cohen et al., U.S. Patent No. 5692152 as applied to Claim 1, and further in view of Crouch et al., U.S. Patent No. 5592493. McClure further teaches the apparatus of claim 1 wherein the logic is a plurality of scan chains (column 10 lines 1-2), but does not teach a test access port to accept automatic test pattern generation (ATPG) patterns. But in an analogous art, Crouch et al. tests a cache (column 7 lines 5-10) using a test access port (column 2 lines 5-13), using ATPG patterns (column 2 lines 51-65). It would have been obvious to modify the apparatus of McClure by providing a TAP such as the one taught by Crouch et al. in order to utilize

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ATPG patterns. And Crouch et al., in column 1 lines 10-30, recites a need to efficiently test and to access components such as a cache by using this invention. One with ordinary skill in the art at the time of the invention, motivated by Crouch et al., would combine the references to use ATPG in testing a cache, and so the claim is rejected.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure, U.S. Patent No. 5666482., in view of Cohen et al., U.S. Patent No. 5692152 as applied to Claim 1, and further in view of the applicant's admitted prior art. McClure further teaches the apparatus of claim 1 wherein the status bit is stored in a six-transistor static random access memory cell (column 10 lines 5-6). The examiner notes that it is well known in the art that a non-volatile device is an SRAM device, and a six-transistor SRAM device is admitted prior art for an SRAM as admitted to by the applicant (Application, page 5 line 19). And in view of the motivation previously stated, the claim is rejected.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure, U.S. Patent No. 5666482, in view of Cohen et al., U.S. Patent No. 5692152 as applied to Claim 1, and further in view of Aipperspach et al., U.S. Patent No. 6181614. McClure teaches the apparatus of claim 1 but does not specifically teach wherein the status bit is stored in a fuse. In analogous art, Aipperspach et al. does teach this feature in column 2 lines 21-22. It would have been obvious to modify the circuit of McClure to include permanently modifiable cells of a fusible type to make changes permanent. And in

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column 2 lines 1-20 the inventor describes the advantage of a self-repair system using persistent repair information. One with ordinary skill in the art at the time of the invention, motivated by Aipperspach et al., would combine the references, and so the claim is rejected.

10. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure, U.S. Patent No. 5666482, in view of Cohen et al., U.S. Patent No. 5692152 as applied to Claim 1, and further in view of Phan, U.S. Patent No. 6634003.

As per Claim 7:

McClure teaches the apparatus of claim 1 but is not specific in teaching that the status bit is a read only bit during normal operation of the system. In an analogous art, Phan does teach this feature. The status bit (FIG.4) is activated only during test and initialization (column 6 lines 8-65), and therefore is read only in normal operation (column 4 lines 11-24). It would have been obvious to make the replacement circuits non-modifiable during normal operation as taught by Phan. And Phan, in column 1 lines 47-61 recites need to improve circuit speed by using the status bit instead of address compares for fault indication during normal operation of a cache. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Phan, would combine the references to improve cache access speed, and thus the claim is rejected.

As per Claim 9:

McClure teaches the apparatus of claim 2, and Phan teaches wherein the PBIST logic can set the status bit during initialization of the cache memory (column 6 lines 8-

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65). And in view of the obviousness and motivation already recited, the claim is rejected.

11. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edmondson et al., U.S. Patent No. 5680544, in view of Phan, U.S. Patent No. 6634003, and further in view of in view of Cohen et al., U.S. Patent No. 5692152.

As per Claim 10:

Edmondson et al. teaches an article comprising: a storage medium having stored thereon instructions (see columns 7 and 8 for example), that, when executed by a computing platform (see Abstract), result in execution of testing a processor's cache memory with a plurality of cache lines (column 3 lines 40-52 and Abstract); generating a test pattern (column 3 line 51); stimulating the cache memory with the test pattern (column 3 lines 49-51), but does not teach writing to at least one status bit for each cache line to indicate whether the cache line contains a defect. In analogous art, Phan does teach this feature, where (see FIG.4) there is writing to at least one status bit for each cache line to indicate whether the cache line contains a defect (column 5 lines 28-56). But Phan fails to teach reading at least one valid bit to indicate whether the cache line is valid. But in the analogous art of Cohen et al., this feature is taught in column 1 lines 56-67. And in view of the obviousness and motivation for Phan and McClure et al. previously recited, the claim is rejected.

As per Claim 11:

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The article of claim 10 wherein the cache memory is either one of a level 0 (L0) cache, level 1 (L1) cache, or level 2 (L2) cache is further taught by Edmondson et al. in column 13 lines 12-13. And in view of the same obviousness and motivation above, the claim is rejected.

As per Claim 12:

The article of claim 10 wherein the status bit is stored in either one of a six-transistor static random access memory cell, a register file cell, or a fuse. Phan, in FIG.4 shows a latch for storage, which in the art is well known as a register file cell. It would have been obvious to one of ordinary skill to equate a latch to a register as is taught by Phan, and to apply the register circuit to the art thusly. And in view of the motivation for Phan above, the claim is rejected.

As per Claim 13:

The article of claim 10 is limited wherein Phan further teaches the status bit as being a read only bit during normal operation of the cache memory. The status bit (Phan FIG.4) is activated only during test and initialization (Phan column 6 lines 8-65), and therefore is read only in normal operation (Phan column 4 lines 11-24). And in view of the obviousness and motivation for Phan above, the claim is rejected.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

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§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.


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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John P Trimmings
Examiner
Art Unit 2133

jpt



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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Changes approved 5/17/05 JPL

Blakely, Sokoloff, Taylor & Zafman LLP

(503) 439-8778

Title: A METHOD AND APPARATUS FOR FLEXIBLE MEMORY FOR
DEFECT TOLERANCE

1st Named Inventor: Suresh Kottapalli

Express Mail No.:

Sheet: 1 of 2

Docket No.: 42390P12494

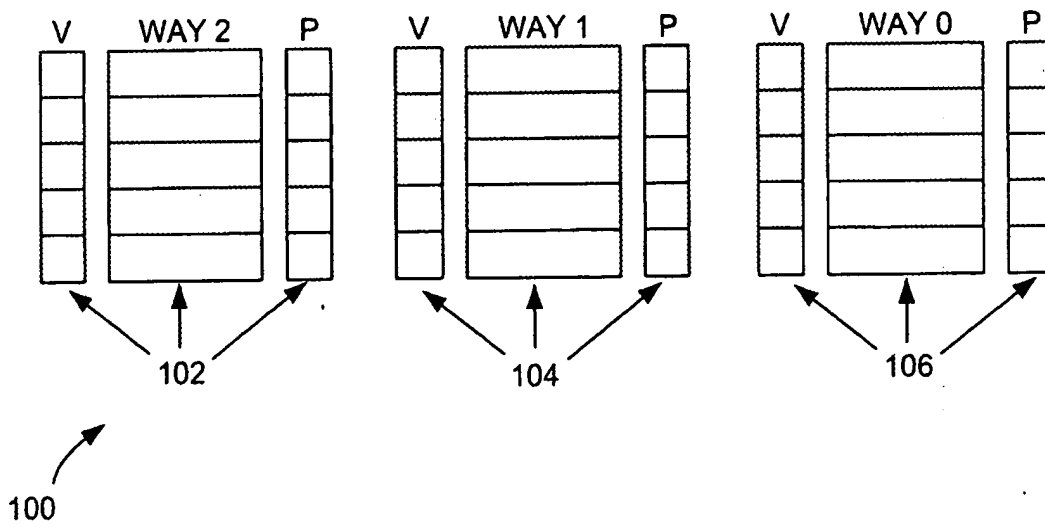


Fig. 1

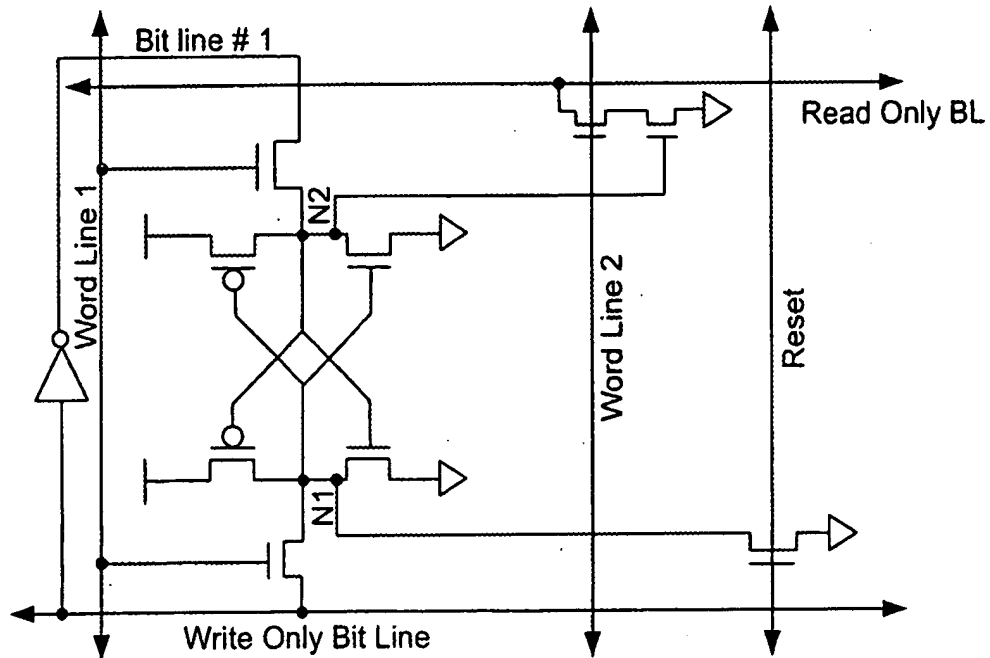
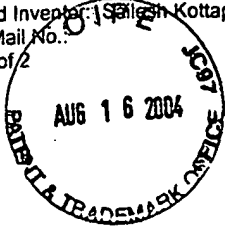


Fig. 2